Ordering number: EN505G

Monolithic Linear IC



No.505G

LA3361

PLL FM MULTIPLEX STEREO DEMODULATOR

Use

The LA3361, PLL FM multiplex stereo demodulator, is designed for low supply voltage-use appliance such as portable radio or car stereo.

Features

1. Wide supply voltage range down to low supply voltage: 3V min.
2. Operation of forced monaural (IF muting) or VCO stopping by only one pin.
   Depending on supply voltage:
   0.7V < V9 < 2.1V: forced monaural (IF muting)
   V9 > 2.1V: VCO stopping
3. Good ripple rejection.
4. High level of lamp turning-on sensitivity: 7mV.
5. With separation control pin.
6. High gain.
7. Less current consumption: 8.5mA typical.

Maximum Ratings at Ta=25°C

				unit
Maximum Supply Voltage	V_{CCmax}	pin 6-7	16	V
		pin 1-7	16	V
Lamp Driving Current	I_L		40	mA
Allowable Power Dissipation	P_{dmax}	Ta≦50°C	400	mW
Operation Temperature	Topr		-20 to +70	°C
Storage Temperature	Tstg		-40 to +125	°C

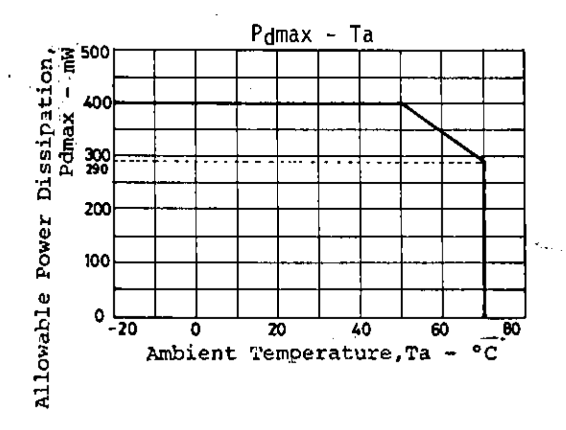
Recommended Operating Conditions at Ta=25°C

			unit
Recommended Supply Voltage	V_{CC}	6	V
Input Signal Voltage	v_i	100 to 200	mV

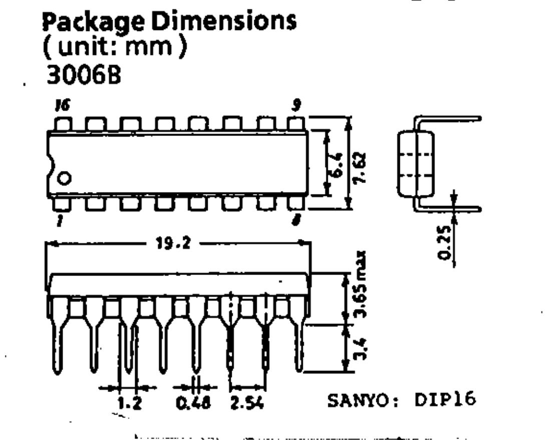
Operating Characteristics at Ta=25°C, V_{CC}=6V, R_L=3.3kohms, input=100mV, L+R=90%, pilot=10%, f=1kHz:

			min	typ	max	unit
Quiescent Current	I_{CCO}			8.5	12.0	mA
Input Resistance	r_i		15k	20k		ohm
Channel Separation			35	45		dB
Total Harmonic Distortion	THD	stereo, sub		0.2	0.7	%
Output Voltage	v_O	v_i=100mV	66	85	115	mV
Channel Balance				0.5	1.5	dB

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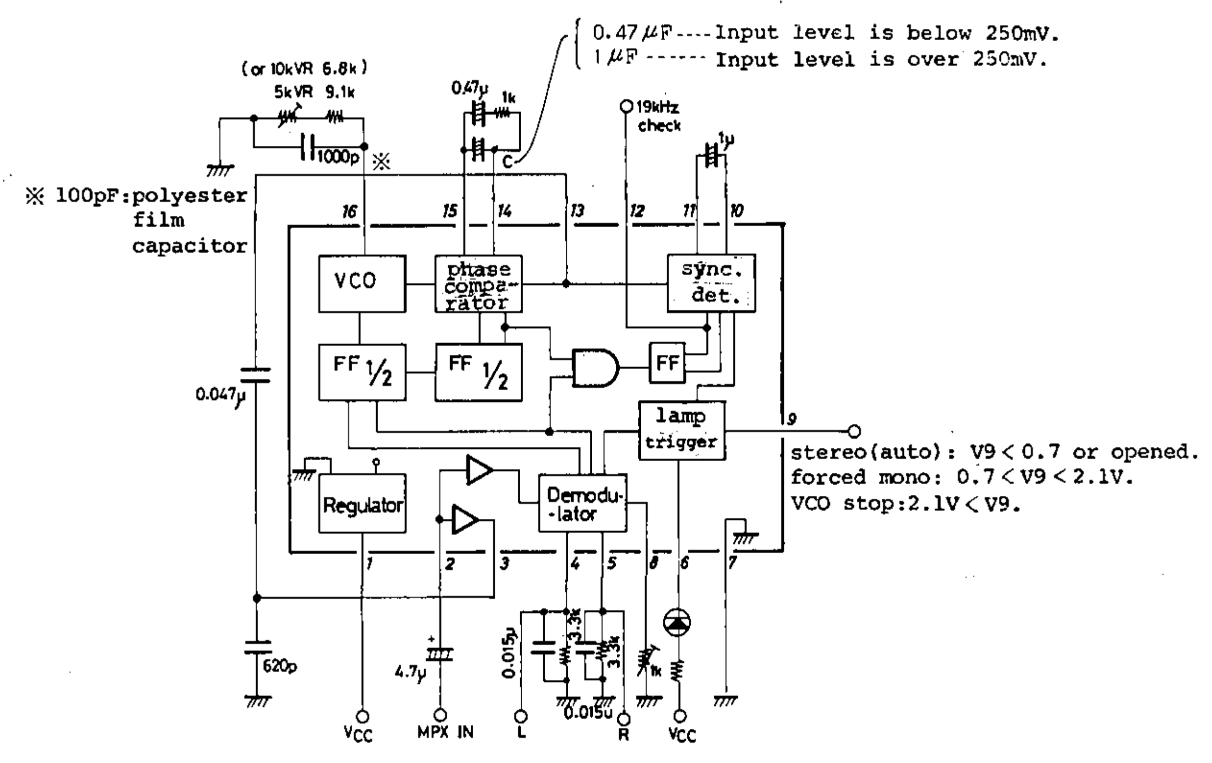
Package Dimensions
(unit: mm)
3006B



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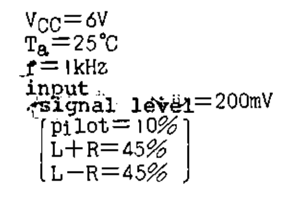
			min	typ	max	unit
Lamp Turn-on Level	V_L	L+R=90%,pilot=10%		65		mV
Hysteresis	hy			3.5	6.0	dB
Capture Range	CR			±2.5		%
Allowable Input Level	vi	THD=2%		450		mV

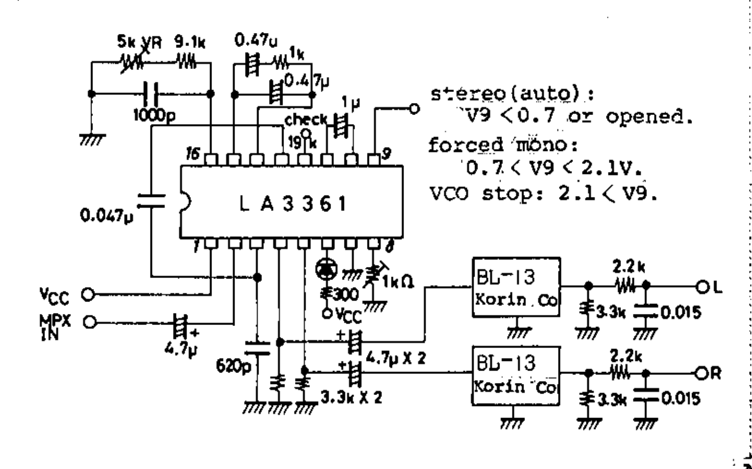
Equivalent Circuit Block Diagram and Peripheral Circuit

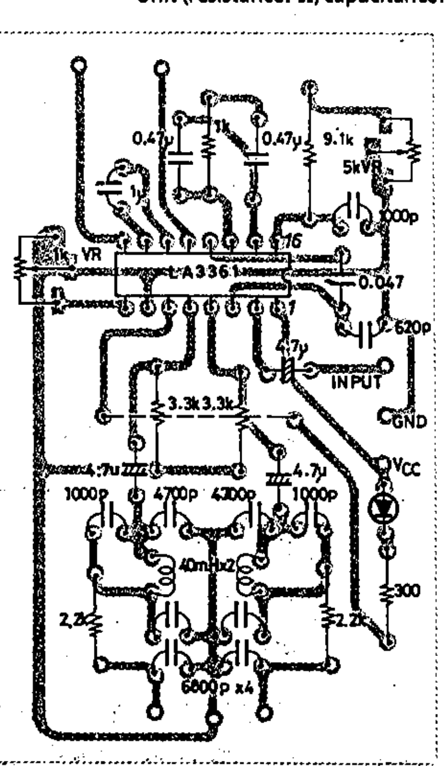


Unit (resistance: Ω, capacitance: F)

Sample Application Circuit

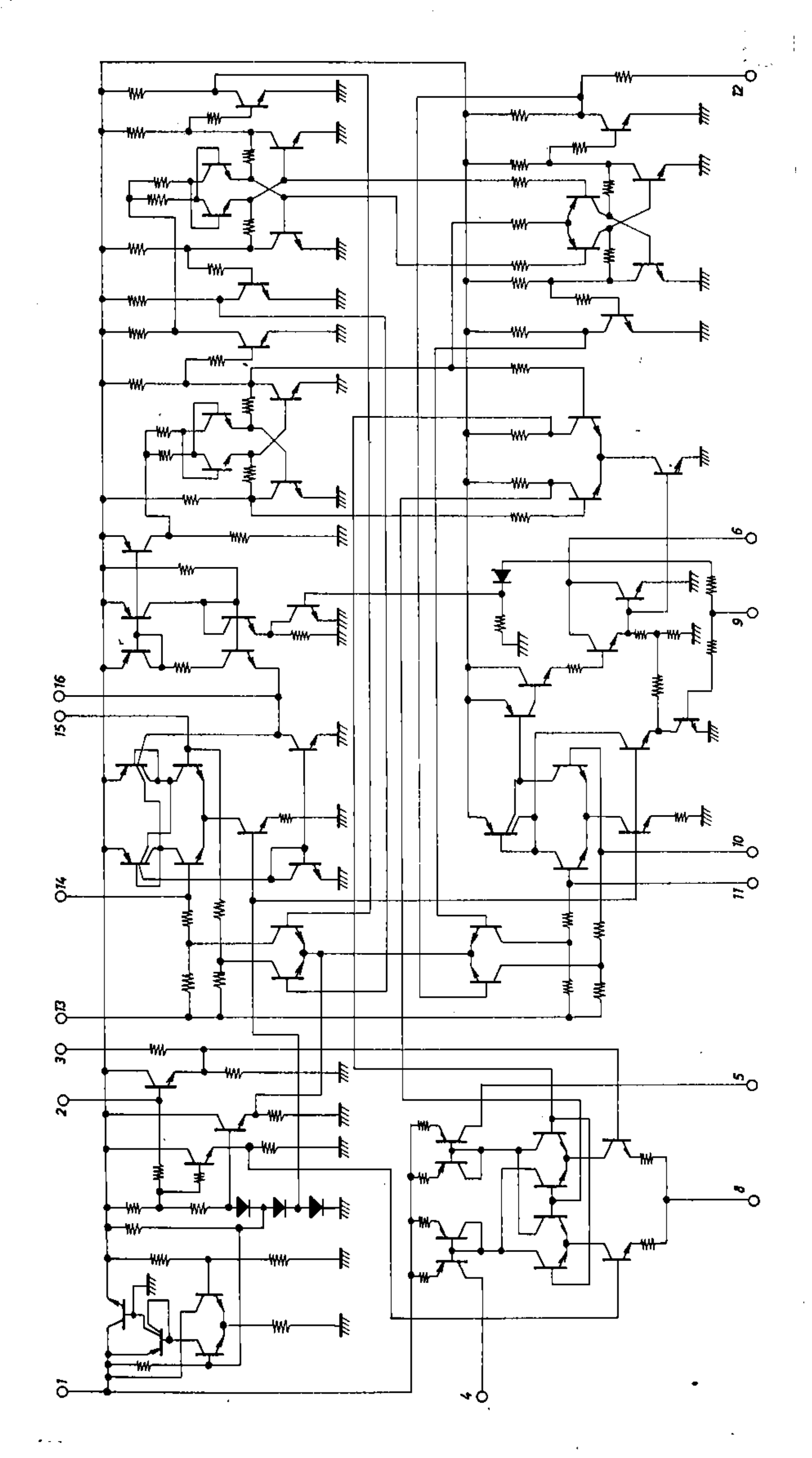


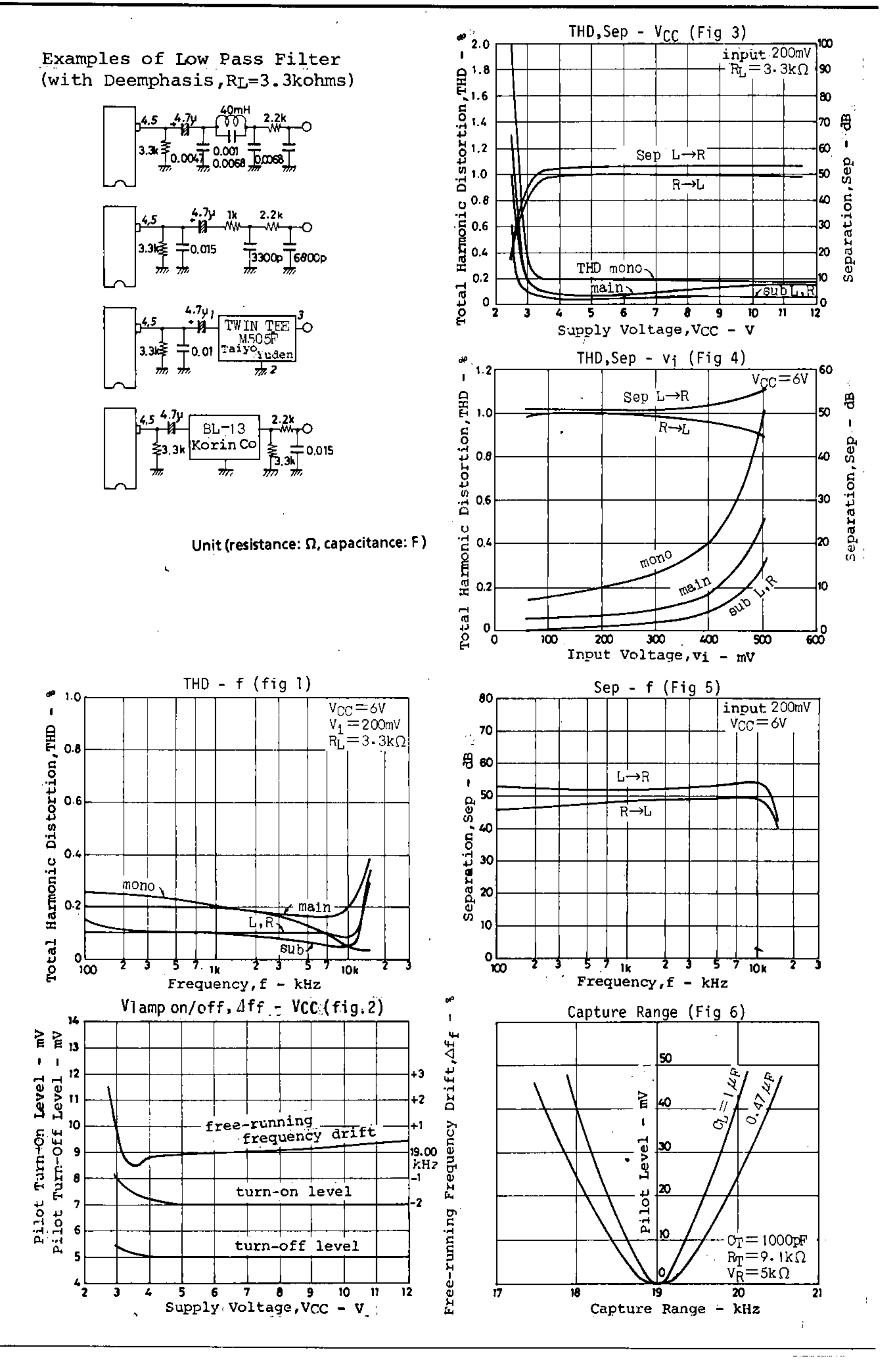




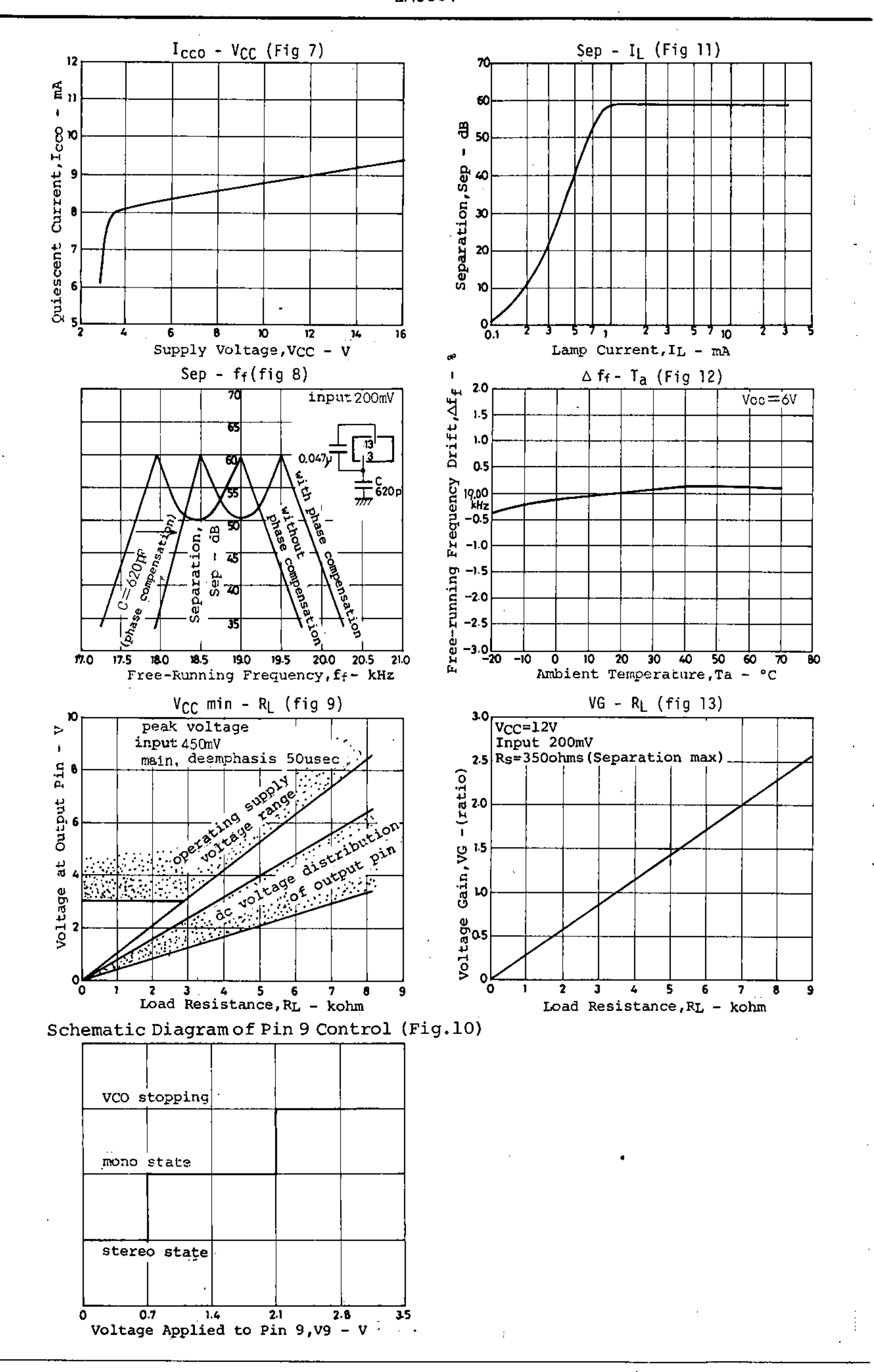
An Example of Printed Pattern Using LC Filter (Cu-foiled area, 50x82mm²)

Equivalent Circuit





Examples of Low Pass Filter
(with Deemphasis, RL=3.3kohms)
Unit (resistance: Ω, capacitance: F)
THD, Sep - VCC (Fig 3)
input 200mV
RL=3.3kΩ
Sep L→R
R→L
THD mono
main
sub L, R
Total Harmonic Distortion, THD - %
Separation, Sep - dB
Supply Voltage, VCC - V
THD, Sep - vi (Fig 4)
VCC=6V
mono
main
sub L, R
Input Voltage, vi - mV
THD - f (fig 1)
VCC=6V
Vi=200mV
RL=3.3kΩ
Frequency, f - kHz
Sep - f (Fig 5)
input 200mV
VCC=6V
L→R
R→L
Vlamp on/off, Δff - VCC (fig. 2)
free-running frequency drift
turn-on level
turn-off level
Pilot Turn-On Level - mV
Pilot Turn-Off Level - mV
Free-running Frequency Drift, Δff - %
Capture Range (Fig 6)
CL=1μF
0.47μF
CT=1000pF
RT=9.1kΩ
VR=5kΩ
Pilot Level - mV
Capture Range - kHz



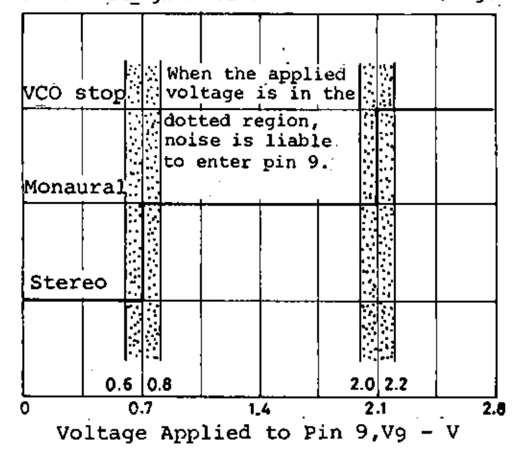
Icco - VCC (Fig 7)
Quiescent Current, Icco - mA
Supply Voltage, VCC - V
Sep - IL (Fig 11)
Separation, Sep - dB
Lamp Current, IL - mA
Sep - ff (fig 8)
input 200mV
0.047μ
C 620p
C=620pF (phase compensation)
Separation, Sep - dB
without phase compensation
with phase compensation
Free-Running Frequency, ff - kHz
Δ ff - Ta (Fig 12)
Vcc=6V
Free-running Frequency Drift, Δff - %
19.00 kHz
Ambient Temperature, Ta - °C
VCC min - RL (fig 9)
peak voltage
input 450mV
main, deemphasis 50usec
operating supply voltage range
dc voltage distribution of output pin
Voltage at Output Pin - V
Load Resistance, RL - kohm
VG - RL (fig 13)
VCC=12V
Input 200mV
Rs=350ohms (Separation max)
Voltage Gain, VG - (ratio)
Load Resistance, RL - kohm
Schematic Diagram of Pin 9 Control (Fig.10)
VCO stopping
mono state
stereo state
Voltage Applied to Pin 9, V9 - V

Proper cares in using the IC

(1) Pin 9-used control

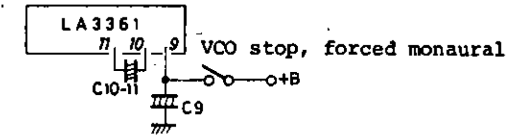
Pin 9 is for stereo/monaural selection and VCO stop. When a voltage of less than 0.7V is applied to pin 9 or pin 9 is grounded or brought into the open state, the stereo (automatic) mode is entered. When a voltage of more than 2.1V is applied to pin 9, the VCO stops operating and the stereo indicator is prevented from malfunctioning. Therefore, no external measure against malfunction is required. When applying a voltage to pin 9, the following should be noted. An applied voltage of approximately 0.7V or 2.1V causes the internal transistors to enter the active region and hum or noise is liable to enter pin 9. Therefore, for example, the applied voltage must be set to an intermediate voltage such as 0V, 1.4V, 2.8V.

Schematic Diagram of Pin 9 Control (Fig.14)



Voltage Applied to Pin 9,V_9 – V

When the VCO stop mode caused by application of a voltage to pin 9 is released, the stereo indicator may be turned ON momentarily. This phenomenon is liable to occur if the value of the capacitor across pins 10 and 11 is large (C_{10-11}>2 to 3uF). The reason for this is that if the VCO stop mode and forced monaural mode are released simultaneously when the C_{10-11} is charged with the pin 10 side being at "H" level at the VCO stop mode, the trigger circuit is turned ON until the C_{10-11} is discharged. This can be prevented by making the release of the forced monuaral mode a little later than that of the VCO stop mode. For this purpose, the C_9 is connected across pin 9 and GND as shown below so that the voltage on pin 9 drops slowly at the time of release.



C_9>2C_{10-11} is a rule-of-thumb guide for the relation between C_9 and C_{10-11} which prevents the stereo indicator from being turned ON mistakenly.

(2) Loop filter capacitor C_{14-15}

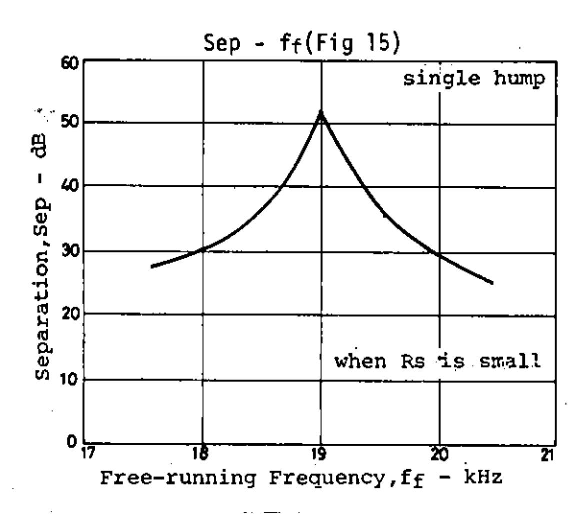
When your set is designed with an input signal level of 250mV or greater, the C_{14-15} is 1uF. The capture range tends to extend with the input level. When your set is designed with a high input signal level of 250mV or greater, your set is liable to be affected by high-frequency signals or noises. Therefore, the loop filter capacitor (across pins 14 and 15) should be made large to narrow the filter bandwidth. If C_{14-15}=1uF is used in your set with an input signal level of 250mV or greater, the capture range is made a little narrower and your set is hard to be affected by high-frequency signals.

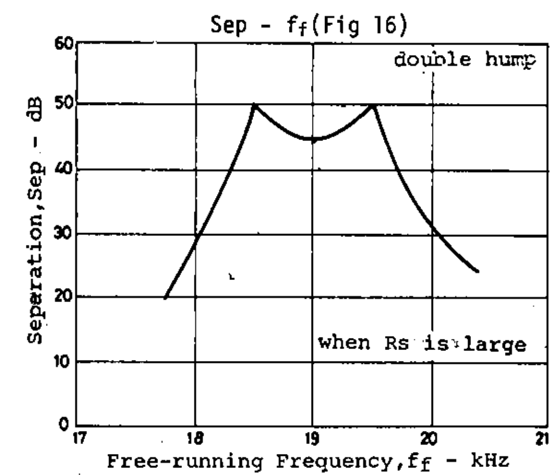
(3) Phase compensation capacitor (See Fig.8.)

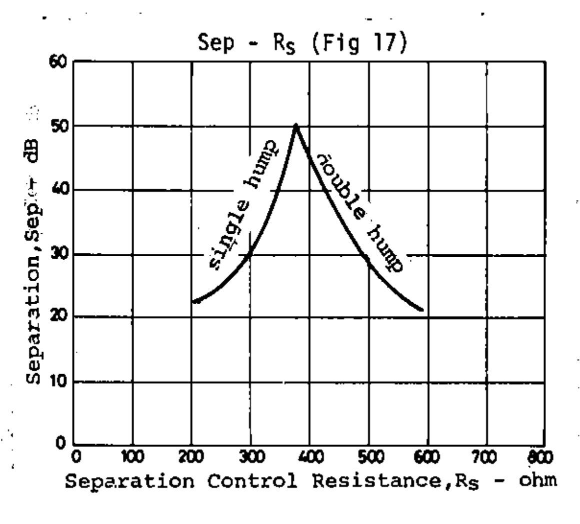
A capacitor of 620pF is connected across pin 3 and GND to compensate the phase lead caused by the decoupling capacitor across pins 3 and 13 and the phase shift caused by the PLL. If no phase compensation capacitor is connected, the center of the separation characteristic plotted against the free-running frequency is off 19.00kHz and the margin for the free-running frequency drift and adjustment error becomes narrow. Therefore, phase compensation should be done.

(4) Separation control

The separation control is done to provide a single or double hump response in the separation vs. free-running frequency characteristic as shown on next page.







As is obvious from the figure shown above, the double hump response has more margin for the free-funning frequency drift. The double hump response is obtained by setting separation control resistance RS to a rather large value. The separation varies with RS as shown above and has peak point at RS≑380kohms give the single hump response. Separation control should be done at a point a little off this peak on the double hump response side. For further details on separation, see the catalog of the LA3350.

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